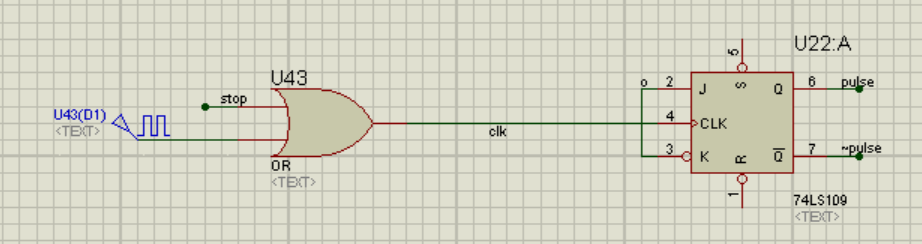
Digisim PS2

In reference to Floyd’s Cycle Finding Algorithm, in the circuit design, Register A refers to the slow pointer and Register B refers to the fast pointer. When the fast pointer moves 2 places, the slow pointer moves only 1 place. This has been achieved by using L1 and L2 loads as input to the registers.

The MUX A has the initial address as input. To load the registers with the initial address, ‘pulse’ is generated by using a JK flip flop.



To check whether cycle exists or not we see for the equality of addresses stored in Register A and B after both fast and slow pointers have moved.

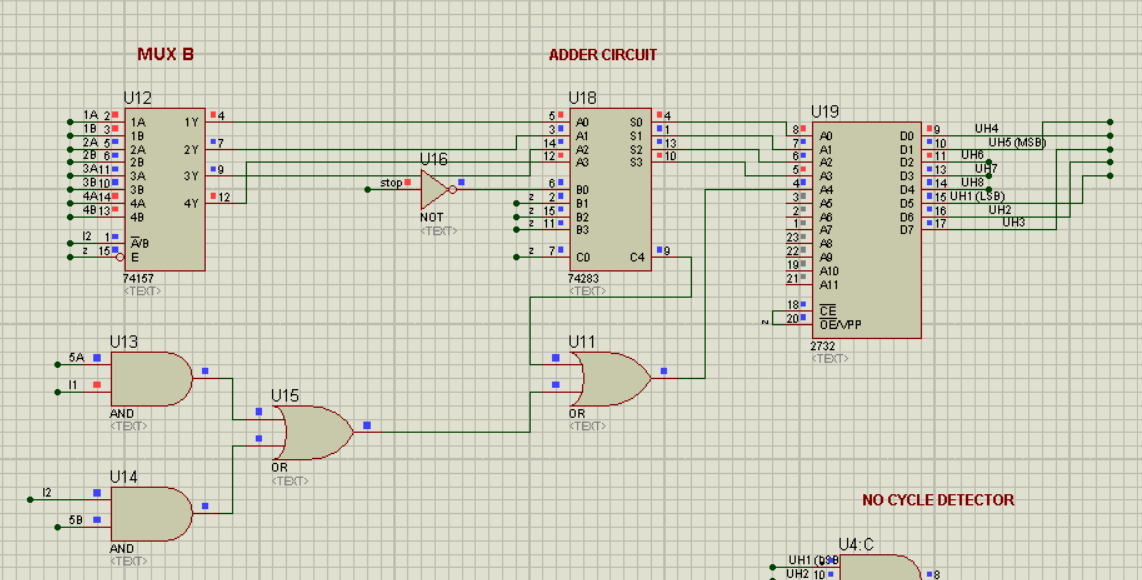
XNOR gates are used to check whether the address stored in both registers is same.L1 and L2 are loads for register A and B. L1 and L2 are generated using counter and ‘pulse’.

When the U20 counter is at 00, the L1(Register A) is activated and when the counter is at 01 and 10 the L2 (Register B) is active. This ensures that the slow pointer moves one unit and the fast pointer moves two units. ‘Pulse’ and ‘equality’ are passed through an XOR gate to get E3 which is used in the MUX A as the selector. ‘Equality’ holds 1 when the pointers are at the same position. It is evaluated by using a 3 input AND gate with L1, equal address comparing logic and a JK flip flop output whose output stays at 1 once the counter achieves 2 (10).

The U3:B D flip flop takes ‘equality’ as input and the outputs Q and Q complement are taken as ‘state 2’ and ‘state 1’. When the equality is achieved then Q becomes 1 and ~Q is passed to set so that output remains constant. ‘state 2’ is input with ‘equality’ into an AND gate.

The output ‘cycle exist’ is passed through AND with the No Cycle Detector circuit output to get ‘stop’. If the ‘stop’ logic is high, then the clock becomes constant, which means no change occurs in the clock.

For unhashing, we have a system consisting of MUX B and Adder Circuit. The MUX B selects from the Register A and Register B output addresses. The adder increments the address by 1 when stop is low and inputs it to the ROM. The output of the ROM is read in the unhashed format by taking the first three outputs (from MSB) and giving them labels for the last three bits (from LSB) for the unhashed address. The other outputs are also labelled accordingly.



COST CALCULATION:

|  |  |  |
| --- | --- | --- |
| Components | Number of components used | Total cost for the component |
| 74LS109 | 2 | 2 |
| 74179 | 2 | 4 |
| 74283 | 1 | 2 |
| 2 input Logic Gates | 32 | 3.2 |
| 3 input Logic Gates | 5 | 1 |
| 7474 | 3 | 3 |
| 74157 | 2 | 4 |
| 2732 | 1 | 75 |
| 74163 | 1 | 2 |
| Clock | 1 | 40 |

The total cost of the design is 136.2